REMARKS

In response to the Official Action mailed July 18, 2002, Applicants amend their application and request reconsideration. In this Amendment, no claims are added and claim 6 is canceled so that claims 1-5 remain pending. No new matter has been added.

Claim 1 is amended to clarify the invention and to correct grammatical errors. Amended claim 1 recites placing a netlist to produce a circuit placement. It is commonly known in the art of automated circuit design that "place," "placing," and "placement" refer to the act of arranging circuit components on a chip or an abstract representation of a chip, as well as the arrangement itself. Thus, one skilled in the art will understand that "placing a netlist" means arranging the components of a circuit, that are represented in the netlist, on a chip or computer simulation of a chip. Likewise, "route" and "routing" refer to the act of arranging interconnections between circuit components, as well as the arrangement itself. One skilled in the art will recognize that "routing a netlist" means mapping the physical interconnections between circuit components. Amended claim 1 now better expresses what is meant by the terms "place" and "route."

Furthermore, amended claim 1 now recites the necessity of the sequence of placement, generating clock trees, and routing. Clock tree generation occurs after the placement of the netlist, which includes the circuit components and delay gates, has occurred. Routing of the netlist occurs after the clock trees have been generated for the circuit placement (see page 4, lines 9-15 of the patent application). Amended claim 1 now recites those sequential steps of this method.

Claim 2 has been amended for clarity. Claim 3 has been amended for clarity, and to elucidate what was meant by "a large region is assured." Amended claim 3 now recites that placing said netlist includes collectively placing a plurality of delay gates in a region where only clock lines and delay gates are disposed, such that the clock lines are not influenced by other lines (see page 15, lines 5-12 of the patent application). Thus, in this region there are no other wirings or elements that will affect the clock lines to produce clock skew.

Claims 1-6 were objected to as informal. The alleged informalities in examined claims 1 and 3 cited by the Official Action are not present in amended claims 1 and 3. The objection to claim 6 is moot, as that claim has been canceled.

Claims 1-6 were rejected as unpatentable over Shinagawa (U.S. Pat. No. 6,053,950). That rejection is respectfully traversed.

Shinagawa does not seek to solve the same problems as the claimed invention. According to Shinagawa, a plurality of standard clock trees prepared as a library are laid out, and flip-flops are then laid out over the standard clock trees. Inevitably, there are unnecessary buffer cells according to the configuration of the circuit and the number of flip-flops. These unnecessary buffer cells are removed to improve the efficiency of the layout (see Abstract and

Figure 1 of Shinagawa). By contrast, the insertion and deletion of buffers according to the claimed invention is performed for adjusting the clock skew among the plurality of clock trees often required in a semiconductor circuit. Thus, clock skew can be easily adjusted without the need for major rerouting.

Regarding claim 1, Shinagawa does not teach or suggest generating clock trees for a circuit placement that satisfy a timing constraint. The clock trees of Shinagawa are retrieved from a library of standard clock trees, and thus clearly cannot be construed as "generated" (see column 2, lines 46-53 and Fig. 1 of Shinagawa). Because the Shinagawa clock trees are standard clock trees, they are obviously not generated for specific circuit placements. Furthermore, the Shinagawa clock trees are retrieved from a library, and thus do not satisfy the sequence of amended claim 1 that recites generating a clock key *after* placement has occurred. Still further, the buffers of Shinagawa are not inserted into the target input; instead, they are included in the standard clock tree, which is placed before the circuit is placed (see column 2, lines 1-3; column 3, lines 11-17; and Fig. 1 of Shinagawa). By contrast, the delay gates of amended claim 1 are inserted into the netlist. In other words, the circuit elements and delay gates are placed together.

Still further, Shinagawa does not teach nor suggest the use of timing constraints to adjust skew. In the present invention, delay gates are deleted from the design to reduce clock skew so that the circuit may satisfy a timing constraint (see page 5, line 20 to page 6, line 6 of the patent application). By contrast, Shinagawa does not teach the use of timing constraints, and, instead, deletes buffers based on their load, or the load of their preceding buffers (see column 3, lines 14-26 of Shinagawa). Because Shinagawa does not teach or suggest numerous limitations of amended claim 1, *prima facie* obviousness has not been established. Accordingly, the rejection of amended claim 1 should be withdrawn.

Regarding amended claims 2 and 3, Shinagawa fails to disclose collectively placing a plurality of delay gates when the netlist is placed. The buffers of Shinagawa are already laid out in a prepared library of standard clock trees (see column 2, lines 1-3; column 3, lines 11-17; and Fig. 1 of Shinagawa). Thus, delay gates are not collectively placed with the netlist. Furthermore, Shinagawa does not disclose placing delay gates in a region, free of other elements, where only delay gates and clock lines are disposed. Accordingly, Shinagawa cannot teach or suggest all of the limitations of claims 2 and 3. Thus, *prima facie* obviousness has not been established, and the rejection should be withdrawn.

Regarding claims 4 and 5, the Official Action incorrectly asserts that Shinagawa teaches not deleting the first and last stages of the delay gates. Shinagawa explicitly teaches deleting the final stage buffer, provided that it satisfies a condition (see column 3, lines 17-20 and 41-43 of Shinagawa). Accordingly, Shinagawa cannot teach or suggest all of the limitations of claims 4

and 5. Thus, *prima facie* obviousness has not been established, and the rejection should be withdrawn.

The rejection of claim 6 is now moot, as that claim has been canceled.

Reconsideration and withdrawal of the rejection, as well as prompt allowance of the pending claims, are appropriate and earnestly solicited.

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JAW/AWF:ves

Attorney Docket No. 400966/SAKAI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

FURUMOTO et al.

Application No. 09/729,088 Art Unit: 2825

Filed: December 5, 2000 Examiner: A. Thompson

For: A METHOD OF DESIGNING SEMICONDUCTOR CIRCUIT AND A SEMICONDUCTOR CIRCUIT DESIGNED USING THIS METHOD

AMENDMENTS TO SPECIFICATION, CLAIMS, AND ABSTRACT MADE IN RESPONSE TO OFFICE ACTION DATED JULY 18, 2002

Amendments to the paragraph beginning at page 7, line 10:

A ~~constrain~~ constraint of timings between the clock trees "to delay an average value of delay values from the starting point to each of the flip-flops in the clock tree 1 from an average value of delay values from the starting point to each of the flip-flops in the clock tree 2 by 2~~nm~~ ns (when the starting point is the output pin of the PLL)"~~is placed~~.

Amendments to existing claims:

1. (Twice Amended) A method of designing a semiconductor circuit having clock trees, the method comprising ~~the steps of~~:

generating a netlist;

inserting a plurality of delay gates ~~onto~~ into said netlist;

~~place~~ placing said netlist to produce a circuit placement;

generating clock trees for said circuit placement ~~which~~ that satisfy a ~~constraint of timing in said clock trees~~ timing constraint;

~~route~~ routing said netlist after generation of said clock trees;

manually adjusting skew between said clock trees by deleting some of said delay gates inserted based on the ~~constraint of~~ timing constraint between said clock trees;

examining the skew between clock trees;

determining whether the ~~constraint of~~ timing constraint is satisfied; and

making a minimum change in the ~~place~~ placing and ~~route~~ routing ~~in association with insertion of~~ when said delay gates are inserted.

2. (Amended) The method of designing a semiconductor circuit according to claim 1, wherein ~~in the step of place,~~ placing said netlist includes collectively placing a plurality of delay gates ~~on said clock line are collectively placed~~.

3. (Amended) The method of designing a semiconductor circuit according to claim 1, wherein ~~in the step of place,~~ placing said netlist includes collectively placing a plurality of delay gates ~~on said clock line are collectively placed and a large region is assured~~ in a region free of lines, other than clock lines, and free of gates, other than delay gates, so that clock lines are not influenced by other lines.

4. (Twice Amended) The method of designing a semiconductor circuit according to claim 2, wherein in ~~the step of~~ manually adjusting skew between trees, said delay gates at first and last stages among said delay gates inserted are not regarded as targets to be deleted.

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PENDING CLAIMS AFTER AMENDMENTS MADE IN RESPONSE TO OFFICE ACTION DATED JULY 18, 2002

1. A method of designing a semiconductor circuit having clock trees, the method comprising :

generating a netlist;

inserting a plurality of delay gates into said netlist;

placing said netlist to produce a circuit placement;

generating clock trees for said circuit placement that satisfy a timing constraint;

routing said netlist after generation of said clock trees;

manually adjusting skew between said clock trees by deleting some of said delay gates inserted based on the timing constraint between said clock trees;

examining the skew between clock trees;

determining whether the timing constraint is satisfied; and

making a minimum change in the placing and routing when said delay gates are inserted.

2. The method of designing a semiconductor circuit according to claim 1, wherein placing said netlist includes collectively placing a plurality of delay gates.

3. The method of designing a semiconductor circuit according to claim 1, wherein placing said netlist includes collectively placing a plurality of delay gates in a region free of lines, other than clock lines, and free of gates, other than delay gates, so that clock lines are not influenced by other lines.

4. The method of designing a semiconductor circuit according to claim 2, wherein in manually adjusting skew between trees, said delay gates at first and last stages among said delay gates inserted are not regarded as targets to be deleted.

5. The method of designing a semiconductor circuit according to claim 3, wherein in manually adjusting skew between trees, said delay gates at first and last stages among said inserted delay gates inserted are not targets to be deleted.